

Accumulate Repeat Accumulate Codes

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Abstract

In this paper we propose an innovative channel coding scheme called "Accumulate Repeat Accumulate codes" (ARA). This class of codes can be viewed as serial turbo-like codes, or as a subclass of Low Density Parity Check (LDPC) codes, thus belief propagation can be used for iterative decoding of ARA codes on a graph. The structure of encoder for this class can be viewed as precoded Repeat Accumulate (RA) code or as precoded Irregular Repeat Accumulate (IRA) code, where simply an accumulator is chosen as a precoder. Thus ARA codes have simple, and very fast encoder structure when they representing LDPC codes. Based on density evolution for LDPC codes through some examples for ARA codes, we show that for maximum variable node degree 5 a minimum bit SNR as low as 0.08 dB from channel capacity for rate 1/2 can be achieved as the block size goes to infinity. Thus based on fixed low maximum variable node degree, its threshold outperforms not only the RA and IRA codes but also the best known LDPC codes with the same maximum node degree. Furthermore by puncturing the accumulators any desired high rate codes close to code rate 1 can be obtained with thresholds that stay close to the channel capacity thresholds uniformly. Iterative decoding simulation results are provided. The ARA codes also have projected graph or protograph representation, that allows for high speed decoder implementation.

Topic area: Turbo and LDPC codes

Key words: Turbo-like codes, LDPC codes, iterative decoding on graphs, density evolution, protographs

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I. INTRODUCTION

Low Density Parity Check (LDPC) codes were proposed by Gallager [1] in 1962. After introduction of turbo codes by Berrou et al [2] in 1993, researchers revisited the LDPC codes, and extended the work of Gallager. During 1962 to 1993, Tanner [3] in 1981 was the only one who paid attention to the work of Gallager and made some contribution. After 1993 over 500 contributions have been made to LDPC codes see for example [12], [14], [15], [5], [16], [17] and references there.

Recently RA [6] and IRA [7] codes, as simple subclasses of LDPC codes with fast encoder structure, were proposed. As turbo-like codes this class can also be considered as a serial concatenated code class [19]. Classical RA codes, in addition to simplicity, have reasonably good performance with iterative decoding threshold within 1 dB of capacity for rates less than or equal to 1/3. RA codes use fixed repetition for input bits. On the other hand, IRA codes inspired by RA and irregular LDPC [4] codes have irregular repetition for input bits. For IRA codes, node degree distribution can be optimized to achieve low thresholds. To achieve very low threshold for IRA, as for LDPC codes, maximum repetition for some portion of input bits can be very high. These recent results on RA and IRA codes, which have fast encoders, motivated us to find a way to enhance the performance of these class of codes and RA codes in particular. Researchers in [9], tried to improve the input-output extrinsic SNR behavior of the outer convolutional codes in serial concatenation in low extrinsic SNR region to lower SNR threshold of serial concatenation by using repetition of certain bits of the outer code. On the other hand if a repetition code is used as an outer code such as in RA codes, one should try to improve the input-output extrinsic SNR behavior at the high extrinsic SNR region, since the input-output extrinsic SNR behavior of repetition codes are excellent in the low extrinsic SNR region. We discovered that an accumulator as a rate-1 precoder applied before the repetition code will improve the performance. Before elaborating on the role of accumulator as a precoder for RA codes and graph representation of ARA codes, we use the definition of projected graph introduced in [10], [11], [13] for implementation of the decoder for LDPC codes which shows that if an LDPC code can be represented by a smallest base-graph (projected graph) then high speed implementation of the decoder will be more feasible. Similar definition also is provided in [8] for base-graph which was called protograph. This definition also facilitates the minimal graph representation for overall graph description of LDPC codes. In fact we will show that ARA codes have such projected graph or protograph representation which is another added value.

A protograph [8] is a Tanner graph with a relatively small number of nodes. A protograph $G = (V, C, E)$ consists of

a set of variable nodes V , a set of check nodes C , and a set of edges E . Each edge $e \in E$ connects a variable node $v_e \in V$ to a check node $c_e \in C$. Parallel edges are permitted, so the mapping $e \rightarrow (v_e, c_e) \in V \times C$ is not necessarily 1:1. As a simple example, we consider the protograph shown in Fig. 1 (b). This graph consists of $|V| = 4$ variable nodes and $|C| = 3$ check nodes, connected by $|E| = 9$ edges. The four variable nodes in the protograph are denoted by types 0, 1, 2, 3, and the three check nodes by types 0, 1, 2. By itself, this graph may be recognized as the Tanner graph of an $(n = 3, k = 1)$ LDPC code (in this case, a Repeat and Accumulate code Fig. 1 (a)). In Fig. 1 (b), the variable nodes connected to the channel are shown with dark filled circles. Blank circles are those variable nodes not connected to the channel (i.e. punctured). Check nodes are circles with inside plus sign. We can obtain a larger graph by a copy-and-permute operation. For the details on protographs see [8]. The resulting larger graph is called the derived graph, and the corresponding LDPC code is a protograph code. In general, we can apply the copy-and-permute operation to any protograph to obtain derived graphs of different sizes. This operation consists of first making T copies of the protograph, and then permuting the endpoints of each edge among the T variable and T check nodes connected to the set of T edges copied from the same edge in the protograph. In Fig. 1 (b), the minimum E_b/N_0 threshold of RA code with iterative decoding is also shown.

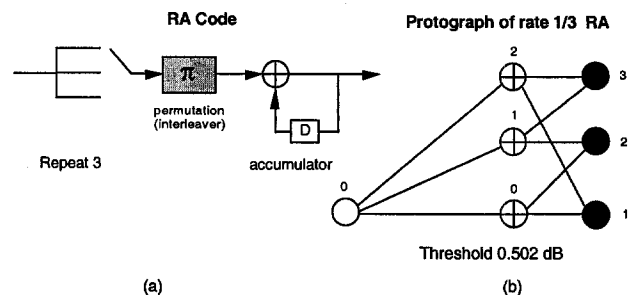


Fig. 1. (a) RA code, (b) Protograph of rate 1/3 RA code with repetition 3

Hui Jin et al [7] proposed Irregular RA (IRA) code which is a serial concatenation of a simple LDPC code with different degree variable nodes (irregular repetition) as an outer code and an accumulator as an inner code to generalize the RA code. The encoder can be implemented by repetition codes, Exclusive OR's, and an accumulator as shown in Fig. 2.

II. PUNCTURED RA AND ALTERNATIVE ENCODING OF IRA CODES

Rate 1/2 classical RA code has high threshold of 3.01 dB. Lower threshold for rate 1/2 RA can be obtained if we puncture the accumulator, provided that the repetition

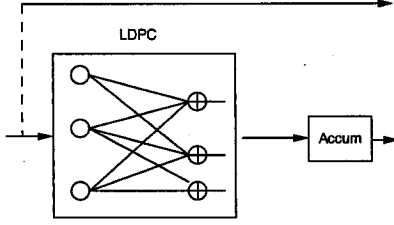


Fig. 2. IRA code

is greater than or equal to 3, and the systematic bits are transmitted through the channel i.e. systematic punctured RA. Based on an equivalent graph of a punctured accumulator, we obtain the protograph of systematic punctured RA with threshold 1.116 dB. This is an improvement close to 2 dB. The systematic punctured RA and its protograph is shown in Fig. 3.

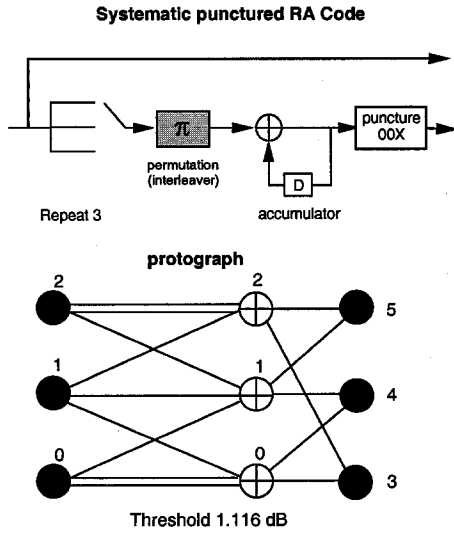


Fig. 3. Systematic punctured RA code

The immediate consequence of this observation suggests an alternative encoding structure for systematic IRA codes by just using irregular repetition, permutation, and punctured accumulator. An example of rate 1/2 systematic IRA, the encoder and the corresponding protograph is shown in Fig. 4. The threshold for this example is 0.990 dB.

III. ACCUMULATE-REPEAT-ACCUMULATE CODES

Let us consider a rate 1/3 serial concatenated code where the outer code is a repetition 3 code. Assume the systematic bits are transmitted to the channel. Alternatively consider the same outer code but the repetition 3 is precoded by an accumulator. Let us compare the extrinsic SNR behavior of these two outer codes using Gaussian density evolution as shown in Fig. 5. As the Gaussian density evolution analysis shows, the use of a rate-1 accumulator dramatically improves the extrinsic SNR behavior of repetition 3 at high extrinsic SNR region. However it slightly deteriorates the behavior of repetition code at very low extrinsic SNR region.

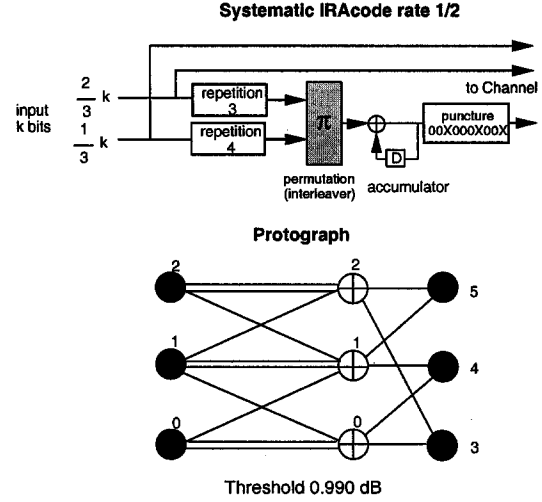


Fig. 4. Systematic IRA

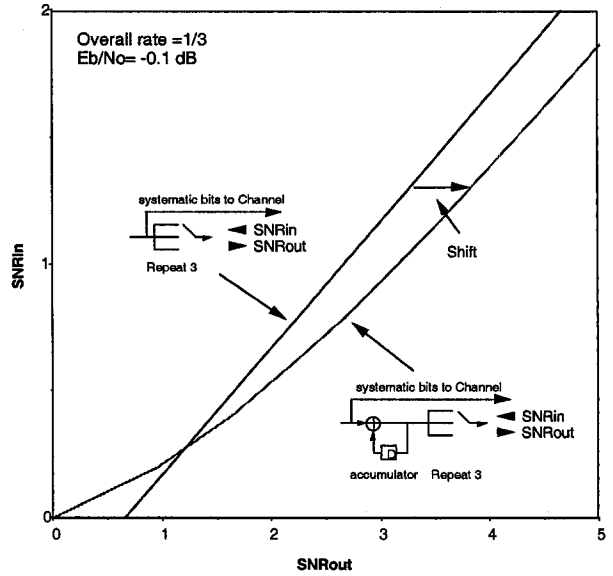


Fig. 5. Gaussian density evolution for repeat 3; with and without precoder

Now let us use a punctured accumulator as an inner code. The periodic puncturing pattern in this example is X0X where 0's indicate the puncturing positions. Since the serial concatenation consists of outer accumulator, middle repetition, and inner accumulator, we call it Accumulate-Repeat-Accumulate (ARA) code. The rate 1/3 ARA, and the extrinsic input-output SNR curves using Gaussian density evolution are shown in Fig. 6.

Gaussian density evolution provide an approximate threshold. Next we present the protograph for this rate 1/3 ARA code, and compute its threshold using density evolution. The protograph and computed threshold of -0.048 dB are shown in Fig. 7. This threshold shows 0.55 dB improvement over classical RA code. If we remove the precoder the threshold will be 0.73 dB. These comparisons will be fair if we fix the maximum variable node degree. Shortly we will show such comparisons with rate 1/2 LDPC codes.

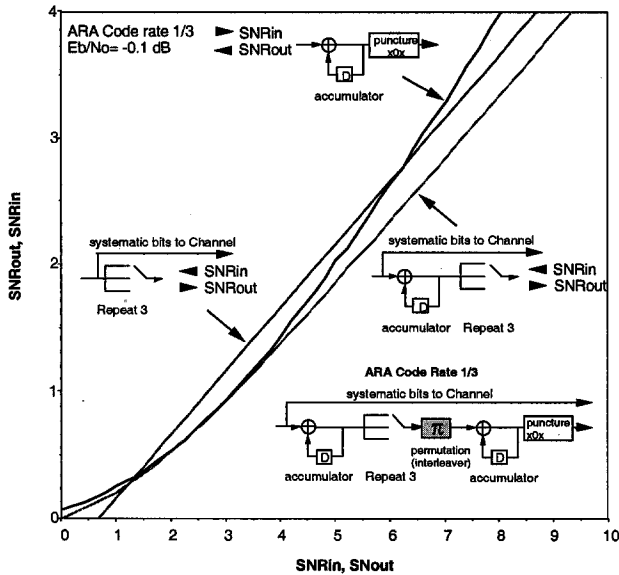


Fig. 6. Gaussian density evolution for rate 1/3 ARA

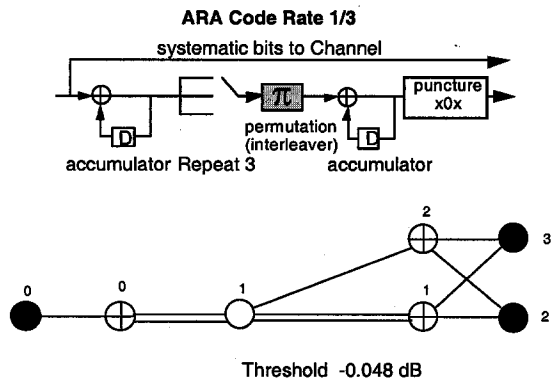


Fig. 7. Rate 1/3 ARA, and the corresponding protograph representation

In a similar way we can construct rate 1/2 ARA code. However, due to more puncturing of the inner accumulator, some portion of input before repetition should not be passed through the precoder to allow the iterative decoding to start. An example of a simple rate 1/2 ARA, its protograph, and the corresponding threshold are shown in Fig. 8. Higher code rate family is obtained by just puncturing the ARA example, and it is shown in Fig. 9.

Another simple example of rate 1/2 ARA with regular repetition is the precoded version of the punctured RA example given previously. The threshold for that punctured RA example was 1.116 dB. The precoded version has threshold of 0.400 dB, and it is shown in Fig. 10. An alternative implementation of encoder using a differentiator also is shown in the Fig. 10 that generates the same protograph. Thus we call the coding scheme "Differentiate-Repeat-Accumulate" code (DRA).

Instead of using regular repetition in ARA, if we use irregular repetition then we refer to it as Irregular ARA or simply IARA code. A simple example of rate 1/2 IARA is the precoded version of the IRA example given previously. The

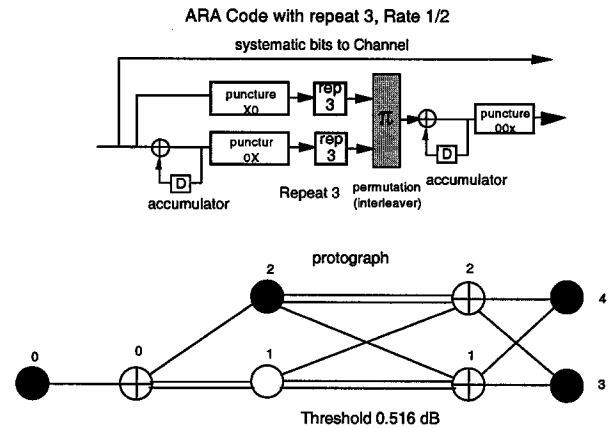


Fig. 8. Rate 1/2 ARA, and the corresponding protograph representation

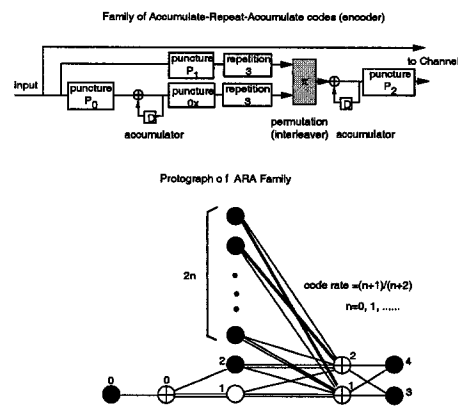


Fig. 9. ARA code family for rates 1/2 to 7/8, encoder, protographs, and table of thresholds in dB

threshold for that IRA example was 0.990 dB. The precoded version has a threshold of 0.364 dB. Higher code rate family is obtained simply by puncturing the IARA example as shown in Fig. 11.

An example of low threshold of 0.264 dB for rate 1/2 ARA code is shown in Fig. 12.

The protograph has maximum degree 5. The best rate 1/2 LDPC with maximum degree 5 in [4] has threshold 0.72 dB. There are few reasons for such difference. In [4], the degree of variable nodes are greater or equal to 2, and punctured variable nodes were not allowed. If we look at protographs of ARA, it contains degree 1 variable nodes and punctured variable nodes. But this is not the main reason. In fact, later Richardson and Urbanke [11], [13] mentioned that the degree 1 variable nodes and punctured variable nodes also can be used in LDPC code design but more than that they mentioned that the so called "multi edge" representation can be used in the LDPC

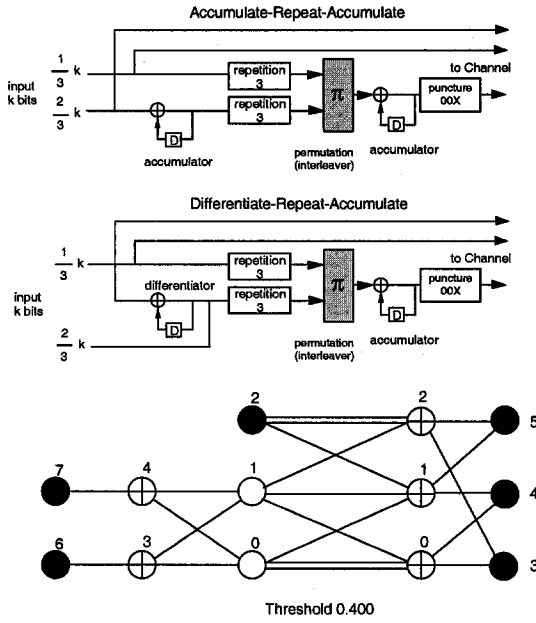


Fig. 10. Rate 1/2 ARA, DRA, and the corresponding protograph representation

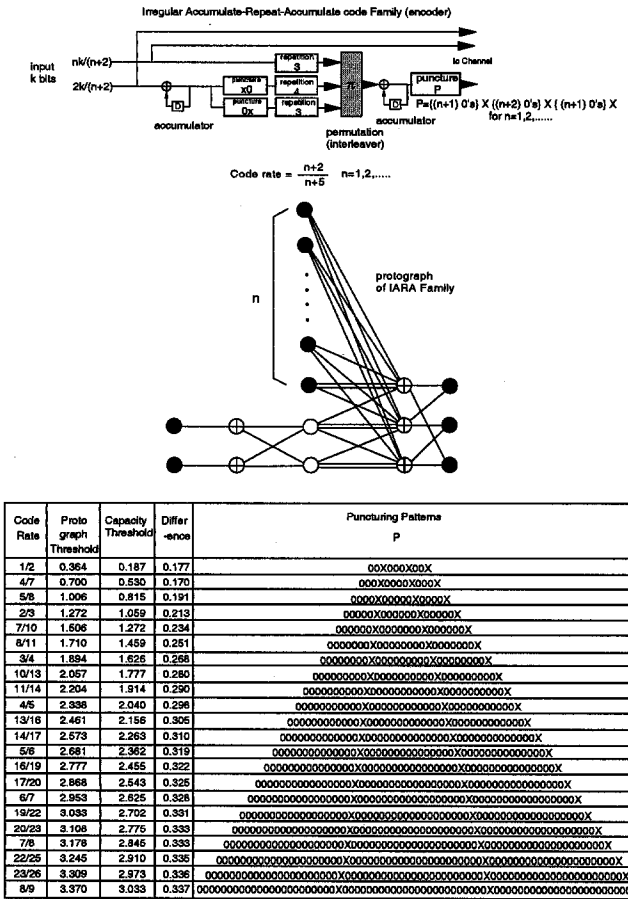


Fig. 11. IARA code family for rates 1/2 to 8/9, encoder, protographs, and table of thresholds in dB

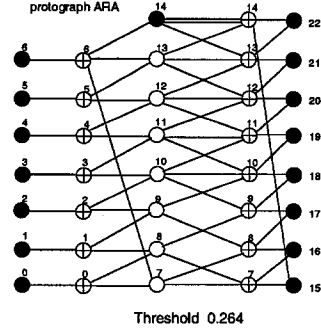


Fig. 12. A rate 1/2 very low threshold ARA protograph

code design. The "multi edge" in ARA code design simply means that the structure of interleaver in ARA codes should be based on edge connections in the ARA protograph between middle variable and inner check nodes (right most check nodes), i.e. between repetition and accumulator. Otherwise a finite threshold may not exist. Finally in this paper preliminary simulation results for random type interleavers (no attempt was used to optimized interleavers) are shown in Fig. 13 for two examples of rate 1/2 ARA codes and compared with a rate 1/2 turbo code with well optimized spread interleaver.

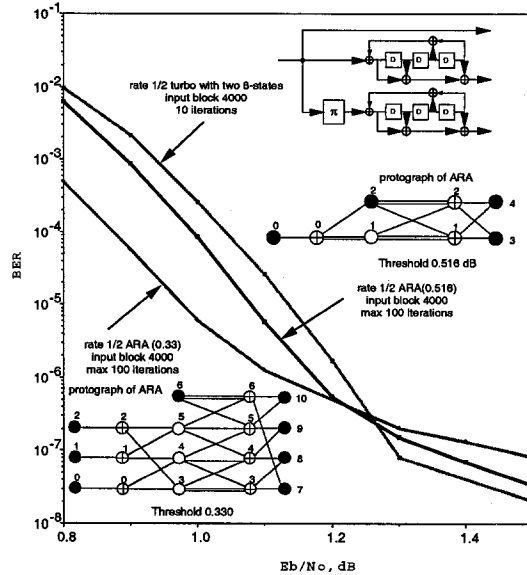


Fig. 13. Simulation results for two examples of rate 1/2 ARAs

IV. CONCLUSION

In this paper we proposed a new channel coding scheme called Accumulate Repeat Accumulate codes (ARA). This class of codes can be viewed as a subclass of Low Density Parity Check (LDPC) codes with fast encoder structure. Based on density evolution for ARA codes, we have shown that for maximum variable node degree 5 a minimum bit SNR as low as 0.08 dB from channel capacity for rate 1/2 can be achieved as the block size goes to infinity. Thus its

threshold outperforms not only the RA and IRA codes but also the best known LDPC codes with the same maximum node degree. A family of high rate codes close to code rate 1 was proposed with thresholds that stay close to the channel capacity thresholds uniformly. Iterative decoding simulation results are provided. The ARA codes also have projected graph or protograph representation, that allows for high speed decoder implementation.

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REFERENCES

- [1] R. G. Gallager, *Low Density Parity Check Codes*. Cambridge, MA: MIT Press, 1963.
- [2] C. Berrou and A. Glavieux, "Near optimum error correcting coding and decoding: Turbo-codes," *IEEE Trans. Commun.*, Vol. 44, pp. 1261-1271, October 1996.
- [3] M. R. Tanner, "A recursive approach to low complexity codes," *IEEE Trans. Inform. Theory*, vol. 27, pp. 533-547, 1981.
- [4] T. Richardson, A. Shokrollahi, and R. Urbanke, "Design of capacity-approaching irregular low-density parity-check codes," *IEEE Trans. Inform. Theory*, vol. 47, pp. 619-637, 2001.
- [5] S.-Y. Chung, D. Forney, T. Richardson, and R. Urbanke, "On the design of low-density parity-check codes within 0.0045 dB of the Shannon limit," *IEEE Communication Letters*, vol. 5, pp. 58-60, 2001.
- [6] D. Divsalar, H. Jin, and R. McEliece, "Coding theorems for Turbo-like codes," in *Proceedings of the 1998 Allerton Conference*, pp. 201-210, 1998.
- [7] H. Jin, A. Khandekar, and R. McEliece, "Irregular repeat-accumulate codes," in *Proc. 2nd International Symposium on Turbo Codes*, pp. 1-8, 2000.
- [8] Jeremy Thorpe, *Low Density Parity Check (LDPC) Codes Constructed from Protographs*, JPL INP Progress Report 42-154, August 15, 2003.
- [9] D. Divsalar, S. Dolinar, and F. Pollara, "Iterative Turbo Decoder Analysis based on Density Evolution," *IEEE Journal on Select Areas in Communications*, Volume: 19 Issue: 5, May 2001, Page(s): 891-907.
- [10] Richardson, et al., "Methods and apparatus for decoding LDPC codes," United States Patent 6,633,856, October 14, 2003.
- [11] T. Richardson, Multi-Edge Type LDPC Codes, presented at the Workshop honoring Prof. Bob McEliece on his 60th birthday (but not included in the proceedings), California Institute of Technology, Pasadena, California, May 24-25, 2002.
- [12] D.J.C. MacKay, R.M. Neal, "Near Shannon limit performance of low density parity check codes," *Electronics Letters*, Vol. 32, Issue 18, 29 Aug. 1996, Page(s) 1645.
- [13] T. Richardson and R. Urbanke, "The Renaissance of Gallager's Low-Density Parity-Check Codes," *IEEE Communications Magazine*, pages 126-131, August 2003.
- [14] M. Luby, M. Mitzenmacher, A. Shokrollahi, and D. Spielman, "Analysis of low density codes and improved designs using irregular graphs," *IEEE Trans. Inform. Theory*, vol. 47, pp. 585-598, 2001.
- [15] T. Richardson and R. Urbanke, "The capacity of low-density parity check codes under message-passing decoding," *IEEE Trans. Inform. Theory*, vol. 47, pp. 599-618, 2001.
- [16] Y. Kou, S. Lin, and M.P.C. Fossorier, "Low-density parity-check codes based on finite geometries: a rediscovery and new results," *IEEE Transactions on Information Theory*, Volume: 47 Issue: 7, Nov. 2001, Page(s): 2711-2736.
- [17] F.R. Kschischang, "Codes defined on graphs," *IEEE Communications Magazine*, Vol. 41, Issue 8, Aug. 2003, Pages 118-125.
- [18] S. Benedetto and G. Montorsi, Unveiling Turbo Codes: Some results on parallel concatenated codes, *IEEE Trans. On Information Theory*, vol. 42, no. 2, March 1996, pp. 409-428.
- [19] S. Benedetto, G. Montorsi, D. Divsalar, and F. Pollara, "Serial concatenation of interleaved codes: Performance analysis, design, and iterative decoding," *IEEE Trans. Info. Theory*, vol. 44, pp. 909-926, May 1998.